ABSTRACT OF THE DISCLOSURE

A plurality of memory cell arrays Array0, Array1, Array2, Array3, Array4, Array5, Array6 and Array7 which can perform a parallel operation are arranged in a later generation chip. Each of the memory cell arrays Array0 and Array4, the memory cell arrays Array1 and Array5, the memory cell arrays Array2 and Array6, and the memory cell arrays Array3 and Array7 constitutes one cell array group. A Pass/Fail signal indicative of success or failure of the operation is outputted in accordance with each cell array group. It is good to make the number of cell array groups equal to the number of memory cell arrays or the number of cell array groups of a precedent generation chip.